MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2017/2018

DCS5158 – COMPUTER ARCHITECTURE

(DIT)

7 MARCH 2018
9.00 a.m. – 11.00 a.m.
(2 Hours)

INSTRUCTIONS TO STUDENT:

1. This question paper consists of 7 pages with 2 sections.
2. Answer **ALL** questions.
3. For **Section A**, shade your answers on the OMR sheet provided.
4. For **Section B**, write your answers in the answer booklet provided.

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SECTION A: MULTIPLE CHOICE QUESTIONS (MCQ) (20 Marks)

Instruction: *Answer **ALL** the questions in this section and shade your answers on the OMR sheet provided.*

1. A _____ is a device that implements a simple Boolean or logical function.
   A. circuit board
   B. memory cell
   C. gate
   D. wafer

2. In 1946, von Neumann and his colleagues began the design of the stored-program computer, referred to as the _____ computer which was the first generation computer that used _____.
   A. ENIAC, vacuum tubes
   B. EDVAC, transistors
   C. IAS, vacuum tubes
   D. IAS, transistors

3. Which of the following structural components of CPU controls the operation of the CPU and decodes the instructions?
   A. ALU
   B. Control unit
   C. Register
   D. Memory

4. Which of the following is the most significant digit of 859.346_{10}?
   A. 8
   B. 9
   C. 3
   D. 6

5. Which of the following is the value of 10100111.0011_2 in decimal representation?
   A. 166.375_{10}
   B. 166.1875_{10}
   C. 167.375_{10}
   D. 167.1875_{10}

6. What is -355_{10} in two's complement with 10-bit representation?
   A. 0101100011_2
   B. 1010011101_2
   C. 1010011100_2
   D. 1010011111_2

Continued...

7. Which of the following is the normalized floating point format for 0.000001110111_2?
   A. 1.110111×2^{-6}
   B. 1.110111×2^{-7}
   C. 1.110111×2^{6}
   D. 1.110111×2^{7}

8. In the following statement, identify *X*.

   The collection of different instructions that the processor can execute is referred to as X.

   A. Operation code
   B. Result operand reference
   C. Next instruction reference
   D. Instruction set

9. Which of the following types of instructions are needed to transfer programs and data into memory and the results of computation back to the user?
   A. I/O instructions
   B. Memory instructions
   C. Test instructions
   D. Branch instructions

10. In the following statement, identify *Y*.

    With Y, instruction execution requires two memory references to fetch the operand in which the first memory reference is to obtain its address and the second is to obtain its value.

    A. Direct addressing
    B. Indirect addressing
    C. Immediate addressing
    D. Register addressing

11. The method of accessing units of data that involves a shared read-write mechanism is referred to as _____ method.
    A. sequential access
    B. random access
    C. associative access
    D. direct access

Continued...

12. _____ is one of the performance parameters that measures the access time plus any additional time required before second access can commence.
    A. Memory cycle time
    B. Transfer rate
    C. Access time
    D. Unit of transfer

13. Which of the following are **TRUE** about bus width?
    I. The address bus width can be specified independently of the data bus width.
    II. The memory and processor buses on Pentium and higher PCs are 64 bits wide.
    III. Older buses like the ISA bus may take two clock cycles to move one bit, halving performance.
    IV. The original ISA bus on the IBM PC was 8 bits wide; the universal ISA bus used now is 16 bits. Other I/O buses (VLB and PCI) are 32 bits wide.

    A. I and II
    B. II and III
    C. I, II and III
    D. I, II and IV

14. Which of the following bus systems is used to designate the source or destination of the data on the bus itself?
    A. Control bus
    B. Data bus
    C. Address bus
    D. System bus

15. Which of the following I/O commands causes the I/O module to obtain an item of data from the peripheral and place it in an internal buffer?
    A. Control
    B. Test
    C. Read
    D. Write

16. There are three techniques for I/O operations. _____ is one of the techniques that allows the data to be exchanged between the processor and the I/O module but it wastes CPU time in periodically checking the status bits of I/O module.
    A. Programmed I/O
    B. Direct memory access
    C. Interrupt-driven I/O
    D. Device communication

Continued...

17. Which of the following I/O techniques is compatible to be used when involved with large volumes of data that are to be transferred?
    A. Direct memory access
    B. Programmed I/O
    C. Interrupt-driven I/O
    D. Memory bus

18. _____ occur when the pipeline, or some portion of the pipeline, must stall because conditions do not permit continued execution.
    A. Pipeline performance
    B. Pipeline hazards
    C. Pipelining
    D. Speedup

19. Which of the following data hazards occurs in which an instruction modifies a register or memory location and hazard occurs if the read takes place before write operation is complete?
    A. Read after write (RAW)
    B. Write after read (WAR)
    C. Write after write (WAW)
    D. Read after read (RAR)

20. Which of the following are the characteristics of Reduced Instruction Set Architectures (RISC)?
    I. One machine instruction per machine cycle
    II. Simple addressing modes
    III. Simple instruction formats
    IV. Register-to-register operations

    A. I, II and III
    B. I, III and IV
    C. II, III and IV
    D. All of the above

Continued...

SECTION B: STRUCTURED QUESTIONS (80 Marks)

Instruction: *Answer **ALL** the questions in this section and write your answers in the answer booklet provided.*

QUESTION 1 (20 Marks)

a) Assume that currently the Program Counter (PC) holds 173H. Execute the first **FIVE (5)** instructions starting from 173 and show the contents of the registers (PC, AC and IR) and any changes made to the memory at the end of each instruction. The original memory contents, relevant instructions with their meanings are given below.

[10 Marks]

Address	Content
173	1824
174	6822
175	5821
176	6823
177	2822
...	...
821	2461
822	2D99
823	1B2F
824	E7A3
...	...

Original memory contents

Instruction	Meaning
0001	Load AC from memory
0010	Store AC to memory
0101	Add to AC from memory
0110	Subtract memory from AC

Partial list of opcodes

b) Use an 8-bit binary representation (2's complement) to show how $-125_{10} + 62_{10}$ is calculated. Verify the result. [5 Marks]

c) Perform the following conversions. All the necessary steps to obtain the answers must be shown.

i. Convert 53545.77214_8 to its hexadecimal equivalent. [3 Marks]
ii. Convert 88933_{10} to its hexadecimal equivalent. [2 Marks]

Continued...

QUESTION 2 (20 Marks)

a) Given the following expression,

$$X = [(P / (E + N * O) - Q] * [D * U - (B - A / U)]$$

i. Convert the expression to postfix notation. [1 Mark]

ii. Write the following machine instructions:

- Zero-address [2 Marks]
- One-address [2 Marks]
- Two-address [2 Marks]

iii. Draw the stack diagrams that illustrate the program execution. [3 Marks]

b) A computer system has a memory architecture made up of main memory of 20GB and cache of 32768KB. In order to perform an efficient mapping function, the main memory is arranged in blocks of 256 bytes.

Draw the address structures for different mapping functions as stated below. Indicate the fields and the number of bits required for each field.

i. Direct Mapping [3.5 Marks]
ii. Thirty Two-Way Set Associative Mapping [3.5 Marks]
iii. Associative Mapping [3 Marks]

QUESTION 3 (20 Marks)

a) State and explain any **THREE (3)** methods of accessing units of data in memory. [6 Marks]

b) Briefly explain the performance parameters of memory as given below.

i. Access time (latency) [2 Marks]
ii. Transfer rate [2 Marks]

c) Describe the following types of the bus in a bus hierarchy.

i. Processor bus (System bus) [2 Marks]
ii. Cache bus (Backside bus) [2 Marks]
iii. Memory bus [2 Marks]

d) Briefly explain the given characteristics of a bus. State the analogy for both characteristics.

i. Bus speed [2 Marks]
ii. Bus bandwidth [2 Marks]

Continued...

QUESTION 4 (20 Marks)

a) List and explain any **THREE (3)** major functions of I/O module in I/O system. [6 Marks]

b) Given **SEVEN (7)** instructions where each instruction has **FIVE (5)** stages (FI, DI, CO, EI and WO) with delays of 4, 4, 4, 6 and 3 seconds for each stage respectively.

i. Draw a timing diagram for instruction pipeline operation. [4 Marks]

ii. Calculate the **total processing time**, **speedup** and **throughput** for the implementation of pipelining and non-pipelining. [10 Marks]
[Note: Please write the formula that is appropriate to use]

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